PhoNoCMap: an Application Mapping Tool for Photonic Networks-on-Chip

Edoardo Fusella, Alessandro Cilardo
Department of Electrical Engineering and Information Technologies, University of Naples Federico II
via Claudio 21, 80125 Napoli, Italy, Email: edoardo.fusella, acilardo@unina.it

***Abstract*—While providing a promising solution for high-performance on-chip communication, photonic networks-on-chip suffer from insertion loss and crosstalk noise, which may severely constrain their scalability. In this paper, we introduce a methodology and a related tool, PhoNoCMap, for the design space exploration of optical NoCs mapping solutions, which automatically assigns application tasks to the nodes of a generic photonic NoC architecture such that the worst-case either insertion loss or crosstalk noise are minimized. The experimental results show significant benefits in terms of insertion loss and crosstalk noise, allowing improved network scalability.**[1]

I. Introduction

The next generation of Multiprocessor Systems-on-Chip will require on-chip communication facilities that cannot be implemented as traditional electronic communication infrastructures [1]. Silicon Photonics appears today a promising solution to handle future communication needs because of ultra-high bandwidth and extremely low power consumption. However, designing an optical on-chip network requires addressing several challenges that have no equivalent in the electronic domain [2]. Insertion loss, i.e. the power loss that a photonic element induces when it is inserted in an optical path, is one of the major limitations affecting the design of a photonic NoC. In fact, the power of an optical signal must be above a certain threshold when arriving at the photodetectors in order to ensure a proper detection. As a consequence, the power injected into the chip must be higher than the photodetector sensitivity plus the worst-case power loss. However, the total power cannot exceed a certain threshold due to the nonlinearities of the silicon material. Multiwavelength signals further exacerbate this problem, since the above considerations apply to each individual wavelength channel. Differently, crosstalk is caused by an unfavorable coupling between optical signals. In multihop photonic NoCs, two different optical signals can induce crosstalk noise to each other when reaching simultaneously a waveguide crossing or a photonic switch. In an ideal setting, optical signals propagate entirely at each waveguide crossing, with no reflection and no crosstalk. Ideal crossing is however unfeasible and hence a small amount of optical power switches into the coupled waveguide.

Such electromagnetic effects should be considered major drivers when designing a photonic NoC architecture, since high values of power loss and/or crosstalk noise may easily result in a network with poor performance, if not inoperable at all. As a major insight of this work, we recognize that application-specific mapping optimization provides an important opportunity to face these problems, in all those scenarios where the application traffic can be statically characterized, which is the case of many embedded applications running on multiprocessor Systems-on-Chip (MPSoCs). While there are currently a large number of high-quality mapping environments available targeting electronic networks-on-chip [3], [4], [5], none can handle the unique physical features that arise when considering chip-scale silicon photonics.

In this paper, we introduce a methodology, and an associated tool, called PhoNoCMap, for the automated design space exploration of mapping solutions in photonic networks. The methodology helps system architects to explore how mapping solutions impact the performance of a particular on-chip optical design and find the best mapping solution for a given application. The tool architecture is fully customizable since new topologies, routing algorithms, optical router architectures, and mapping optimization strategies can be added without any changes in the tool core. In addition, the tool contains built-in analytical models for estimating both power loss and crosstalk noise. Experimental results show that power loss and crosstalk noise can be significantly reduced, enabling improved network scalability.

II. PhoNoCMap

This section briefly describes the PhoNoCMap architecture, followed by a presentation of the modeling and optimization techniques supported by the toolset. The tool primarily consists of four modules, as shown in Figure 1: (1) The input description of the application and architecture, (2) the libraries containing the photonic building blocks and their physical parameters, (3) the architecture models, (4) the design space exploration engine. In the following, these aspects are thoroughly discussed.

A. Inputs

PhoNoCMap addresses the problem of mapping a set of given application tasks, with known traffic characteristics, to the NoC tiles yielding the best SNR or power loss. As a consequence, we need to specify the target application and the NoC architecture. PhoNoCMap takes as input Communication Graphs (CGs) for describing the application communication requirements:

[1]The open-source toolset implementing the PhoNoCMap methodology is accessible at **http://wpage.unina.it/edoardo.fusella/phonocmap/**

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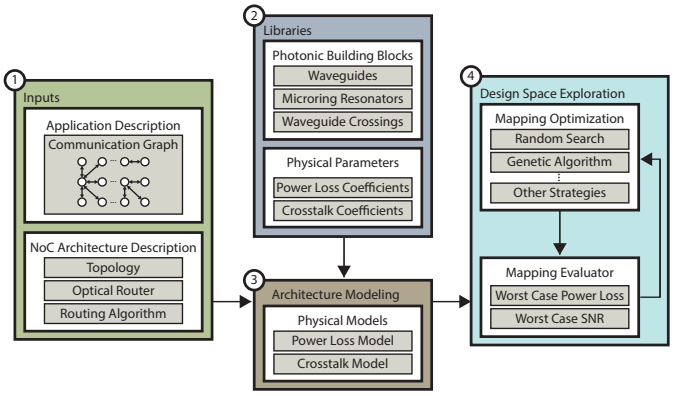

Fig. 1. The PhoNoCMap environment.

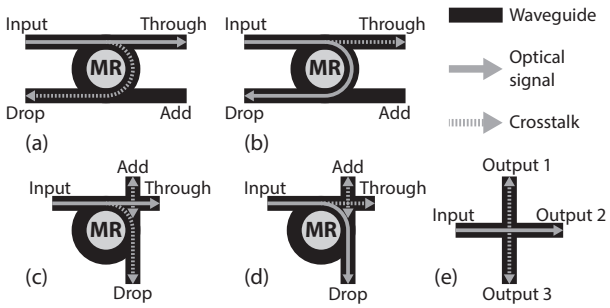

Fig. 2. How optical signal and crosstalk noise propagate through: (a) Parallel PSE in OFF state; (b) Parallel PSE in ON state; (c) Crossing PSE in OFF state; (d) Crossing PSE in ON state; (e) Waveguide Crossing.

Definition 1: A *Communication Graph* $CG = G(C, E)$ is a directed graph where each vertex $c_i \in C$ is a task and $e_{i,j} \in E$ is the edge between tasks c_i and c_j characterizing the communication between them.
Differently, the NoC architecture is described by the topology, the optical router microarchitecture, and the routing algorithm. While PhoNoCMap was initially planned and developed targeting photonic NoC architectures based on direct topologies with dimension order routing, both the underlying models and the tool architecture can be easy extended to any other photonic architecture. As a consequence, all these features are fully customizable by the photonic network designer.

B. Libraries

PhoNoCMap is designed to allow the design space exploration of mapping solutions on photonic networks characterized by different topologies and optical routers, while concurrently enabling a first-order assessment of the physical-layer features. This is realized by exploiting a component library containing the specification of the fundamental network building blocks that will be used for implementing the interconnection network, i.e. the silicon waveguide, the waveguide crossing, and the microring resonator. These building blocks are used for designing traditional photonic switch elements (PSEs), the optical routers, and the topologies. Other components, such as couplers, modulators, detectors, and laser sources are not involved in the mapping process and are thus out of the scope of PhoNoCMap. The photonic devices within this library are characterized by using a model described in more detail in Section II-C. Users of PhoNoCMap can choose to design a network based on the built-in library of devices, or extend the library itself with new photonic building blocks.

C. Modeling

Figure 2 illustrates how optical signals and crosstalk noise propagate for both the parallel PSE (PPSE) and the crossing PSE (CPSE) in ON or OFF resonance and in case of waveguide crossing. The crosstalk noise arises when two optical signals reach simultaneously a waveguide crossing or a PSE. PSEs (Figure 2 a-d) are made up of a microring resonator and two waveguides. When an optical signal injected into the input port matches the wavelength of the microring resonance frequency, then it is coupled into the ring and steered to the drop port (Figure 2(b) and (d)). Otherwise, the signal propagates to the through port (Figure 2(a) and (c)). In [6], the authors present an analytical model for characterizing the power loss and the crosstalk noise. The output power at each port of both the PPSE and CPSE in both the ON and OFF resonance state is evaluated as a function of the input power and the loss/crosstalk coefficients presented in Table I.

TABLE I. LOSS AND CROSSTALK PARAMETERS

Parameter	Notation	Value	Ref.
Crossing loss	L_c	-0.04 dB	[7]
Propagation Loss in Silicon	L_p	-0.274 dB/cm	[8]
Power loss per PPSE in OFF state	$L_{p,off}$	-0.005 dB	[9]
Power loss per PPSE in ON state	$L_{p,on}$	-0.5 dB	[9]
Power loss per CPSE in OFF state	$L_{c,off}$	-0.045 dB	
Power loss per CPSE in ON state	$L_{c,on}$	-0.5 dB	[10]
Crossing's crosstalk coefficient	K_c	-40 dB	[7]
Crosstalk coefficient per PSE in OFF state	$K_{p,off}$	-20 dB	[9]
Crosstalk coefficient per PSE in ON state	$K_{p,on}$	-25 dB	[9]

Compared to previous models in the technical literature [6], we introduced a few modifications and assumptions which do not degrade the accuracy of the model significantly:

- the crosstalk noise on the add port as well as the light that reflects back on the input port are neglected;
- we consider only the first-order crosstalk noise and hence $K_i K_j = 0$, with $K_i, K_j \in \{K_c, K_{p,off}, K_{p,on}\}$;
- we neglected the power loss that affects the crosstalk noise inside the switch where the crosstalk noise is generated. As a consequence, $K_i L_i = K_i$, with $K_i \in \{K_c, K_{p,off}, K_{p,on}\}$ and $L_i \in \{L_c, L_p, L_{p,off}, L_{p,on}, L_{c,off}, L_{c,on}\}$.

Based on the above considerations, the equations presented in [6] are simplified as follows.

$$P_{Tppse,off} = L_{p,off} P_{in} \quad (1a)$$
$$P_{Dppse,off} = K_{p,off} P_{in} \quad (1b)$$
$$P_{Dppse,on} = L_{p,on} P_{in} \quad (1c)$$
$$P_{Tppse,on} = K_{p,on} P_{in} \quad (1d)$$
$$P_{Tcpse,off} = L_{c,off} P_{in} \quad (1e)$$
$$P_{Dcpse,off} = (K_{p,off} + K_c) P_{in} \quad (1f)$$
$$P_{Dcpse,on} = L_{c,on} P_{in} \quad (1g)$$
$$P_{Tcpse,on} = K_{p,on} P_{in} \quad (1h)$$
$$P_{out2} = L_c P_{in} \quad (1i)$$
$$P_{out1} = P_{out3} = K_c P_{in} \quad (1j)$$

Equations (1a) and (1b) and Equations (1d) and (1c) give the output powers at the through and drop ports for the PPSE respectively in the OFF and ON state, while Equations (1e) and (1f) and Equations (1h) and (1g) give the same for the CPSE. Last, Equations (1i) and (1j) give the power detected at the output port of a two-waveguide crossing. Based on the above model, we can to evaluate the worst-case insertion loss IL_{wc}^{dB} as the sum of all the losses in each hop along a path between a source and a destination and the worst-case signal-to-noise ratio as $10\log(P_S/P_N)$, where P_S and P_N are, respectively, the power of the signal and of the crosstalk noise.

D. Design Space Exploration

1) Problem Formulation: Before presenting the design space exploration algorithms, we formulate the mapping problem. The design objective is to map a set of given application tasks, whose traffic characteristics are given in a Communication Graph (CG), to the NoC tiles in the case of a regular topology yielding the best SNR. To this aim, we introduce the topology graph defined in the following.

Definition 2: A *Topology* $X(T, L)$ represents how tiles are connected to each other, where $t_i \in T$ denotes a tile of the NoC and each $l_{i,j} \in L$ is a physical link connecting tiles t_i and t_j.

Using the above graph representation and the communication graph, the problem addressed can be formulated as:
Given a graph CG and a topology X satisfying

$$size(C) \leq size(T) \quad (2)$$

find a mapping function $\Omega : C \rightarrow T$ which maximizes

$$\min\left\{IL_{wc}^{dB} = \max\{IL^{dB}(\Omega(c_i), \Omega(c_j)) \quad \forall e_{i,j} \in E\}\right\} \quad (3)$$

in case of power loss optimization or minimizes

$$\max\{SNR_{wc} = \min\{SNR(\Omega(c_i), \Omega(c_j)) \quad \forall e_{i,j} \in E\}\} \quad (4)$$

in case of crosstalk noise optimization, where IL_{wc}^{dB} and SNR_{wc} are respectively the worst-case insertion loss and the worst-case SNR
such that:

$$\forall c_i \in C, \quad \Omega(c_i) \in T \quad (5)$$
$$\forall c_i \neq c_j \in C, \quad \Omega(c_i) \neq \Omega(c_j) \quad (6)$$

Condition (5) means that each task must be mapped to one tile, while Condition (6) guarantees that each tile will host at most a single task.

Notice that, unlike the other mapping problems addressed in the literature, the crosstalk-aware mapping problem requires at each step a holistic view of the network status since a communication between a source and a destination is affected by a crosstalk noise that depends not only on the mapping of these two nodes, but also on the mapping of all the nodes of the system whose communications generate additional noise.

2) Mapping Optimization Algorithms: The problem of application mapping is NP-hard so practical sizes of mapping problems can only be solved using constructive or transformative heuristics. PhoNoCMap is designed to allow users to choose between a number of mapping optimization algorithms, or extend the library themselves with other algorithms. Currently, three strategies are implemented: a random search (RS), a genetic algorithm (GA), and a purposely developed randomized *priority-based list algorithm* (R-PBLA). The first search algorithm generates randomly a population of a given size and then picks the best individual. Differently, the genetic algorithm creates a fixed-sized population of candidate solutions that, using the crossover and mutation operators, evolves over a number of generations toward better solutions. Last, the priority-based list approach tries, at each step, to make the best move as possible within a list of admitted moves, i.e. the moves consisting on swapping the tasks mapped onto two different tiles. The list is ordered according to the worst-case power loss or SNR associated with any potential move. The algorithm does not allow uphill moves (which cause a temporary cost increase), hence the probability of sticking at a local minimum solution tends to be high. To deal with this problem, when the algorithm finds a local minimum, i.e. a point not having better neighboring solutions, it records the solution and generates another random starting point in the hope of falling in a different region of attraction.

III. Case Studies

The PhoNoCMap methodology described above has been implemented in a Java-based open-source toolset [11] allowing the full reproducibility of the results presented in this paper. We applied PhoNoCMap to eight real streaming video and image processing applications, namely *263dec mp3dec*, which is a H.263 video decoder and MP3 audio decoder (decomposed in 14 tasks); *263enc mp3enc*, which is a H.263 video encoder and MP3 audio encoder (12 tasks); *DVOPD*, which is a dual video object plane decoder (32 tasks); *MPEG-4*, which is a MPEG4 decoder (12 tasks); *MWD*, which is a multi-window display (12 tasks); *PIP*, which is a picture-in-picture application (8 tasks); *VOPD*, which is a video object plane decoder (16 tasks); and *Wavelet*, which is a wavelet transform application (22 tasks). In order to prove that the mapping choice heavily affects the worst-case power loss and signal-to-noise ratio (SNR), we generated randomly 100000 mapping solutions for each application in a mesh-based photonic NoC exploiting the Crux optical router [12] and, using PhoNoCMap, we evaluated the worst-case SNR and power loss related to each mapping

TABLE II. ALGORITHMS COMPARISONS

Application	Mesh						Torus					
	RS		GA		R-PBLA		RS		GA		R-PBLA	
	SNR	Loss	SNR	Loss	SNR	Loss	SNR	Loss	SNR	Loss	SNR	Loss
263dec mp3dec	20.21	-2.04	38.67	-1.52	38.67	-1.52	39.08	-2.12	38.71	-1.68	39.95	-1.60
263enc mp3enc	38.29	-2.04	38.63	-1.94	38.63	-1.59	39.77	-2.12	39.73	-1.97	39.94	-1.75
DVOPD	12.65	-2.79	16.19	-2.15	18.70	-1.85	14.12	-3.18	19.15	-2.23	19.12	-2.04
MPEG-4	19.06	-2.35	19.16	-2.04	20.02	-2.04	20.10	-2.35	20.10	-2.20	21.08	-2.20
MWD	20.24	-1.81	38.63	-1.59	38.63	-1.59	39.72	-1.97	39.28	-1.99	39.95	-1.61
PIP	38.58	-1.90	38.58	-1.68	38.58	-1.68	39.95	-1.86	39.88	-1.70	39.95	-1.70
VOPD	18.66	-2.27	37.83	-1.96	38.67	-1.52	19.24	-2.39	20.29	-2.04	38.59	-1.68
Wavelet	14.58	-2.46	37.95	-2.15	36.86	-1.93	16.29	-3.06	19.65	-2.31	32.52	-2.27

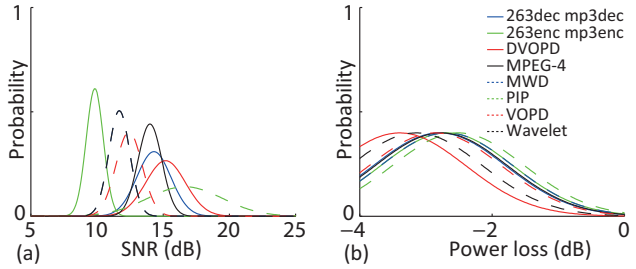

Fig. 3. Probability distribution of the (a) SNR and (b) power loss related to 100000 mapping solutions randomly generated for eight multimedia applications.

solution. Figure 3 shows the probability distribution of SNR and power loss values corresponding to the random generated mapping solutions. It can be easily recognized that the power loss and SNR of the best and worst solution may differ significantly. This experiment points out the high variability of power loss and crosstalk noise according to the different mapping solutions.

Then, we used the different optimization algorithms to find the best mapping solution for each application in a mesh and a torus topology both exploiting the Crux router. The results are summarized in Table II. To guarantee a fair comparison, the running times of the different algorithms are the same. In general, the random search reaches poor mapping solutions in most cases. Only for small-size networks (such as application PIP mapped on a 3×3 topology), it is able to find an appropriate solution. Compared to RS, the genetic algorithm performs better (up to $50-60\%$) when optimizing the crosstalk noise, while, in case of a power loss optimization, this gain is reduced to an average 17%. Differently, our R-PBLA is able to find mapping solutions that outperform on average the solutions found with GA by around 2% and 12% in case of, respectively, mesh and torus topologies for the SNR objective, and between $9-10\%$ for the power loss objective. Notice that both the crosstalk noise and the power loss scale up with the network size: the worst-case values are reached in case of the DVOPD application that is mapped on the bigger topology. Also, applications that are more constrained due to their CGs, such as the MPEG-4 (26 edges), are subjected to a higher power loss and crosstalk noise compared to other applications that are less constrained and mapped on a topology of the same size, such as the 263enc mp3enc (12 edges) and the MWD (12 edges) applications.

IV. CONCLUSIONS

Silicon Photonics appears a promising path to energy-efficient ultra-high bandwidth on-chip communication. However, the mapping of application tasks to NoC tiles is a crucial step in the design of photonic NoCs. In this paper, we introduced a methodology and an associated tool, PhoNoCMap, for the automated design space exploration of mapping solutions for photonic networks, bridging this important gap in the design of photonic NoCs.

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