

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT182** Look-ahead carry generator

Product specification  
File under Integrated Circuits, IC06

December 1990

## Look-ahead carry generator

## 74HC/HCT182

## FEATURES

- Provides carry look-ahead across a group of four ALU's
- Multi-level look-ahead for high-speed arithmetic operation over long word length
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT182 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT182 carry look-ahead generators accept up to four pairs of active LOW carry propagate ( $\overline{P}_0, \overline{P}_1, \overline{P}_2, \overline{P}_3$ ) and carry generate ( $\overline{G}_0, \overline{G}_1, \overline{G}_2, \overline{G}_3$ ) signals and an active HIGH carry input ( $C_n$ ). The devices provide

anticipated active HIGH carries ( $C_{n+x}, C_{n+y}, C_{n+z}$ ) across four groups of binary adders.

The "182" also has active LOW carry propagate ( $\overline{P}$ ) and carry generate ( $\overline{G}$ ) outputs which may be used for further levels of look-ahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$

$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$

$$\overline{G} = \overline{G}_3 + \overline{P}_3 \overline{G}_2 + \overline{P}_3 \overline{P}_2 \overline{G}_1 + \overline{P}_3 \overline{P}_2 \overline{P}_1 \overline{G}_0$$

$$\overline{P} = \overline{P}_3 \overline{P}_2 \overline{P}_1 \overline{P}_0$$

The "182" can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V			
	$\overline{P}_n$ to $\overline{P}$		11	14	ns
	C <sub>n</sub> to any output		17	21	ns
	$\overline{P}_n$ or $\overline{G}_n$ to any output		14	17	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	50	50	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>

For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

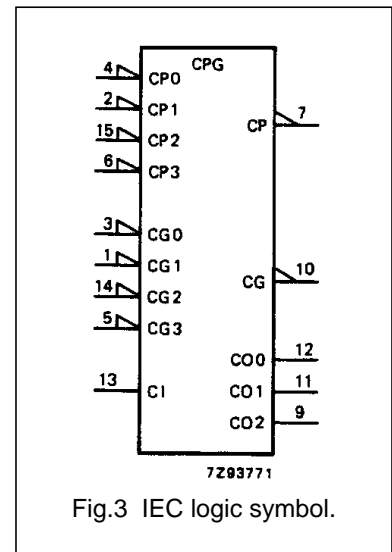
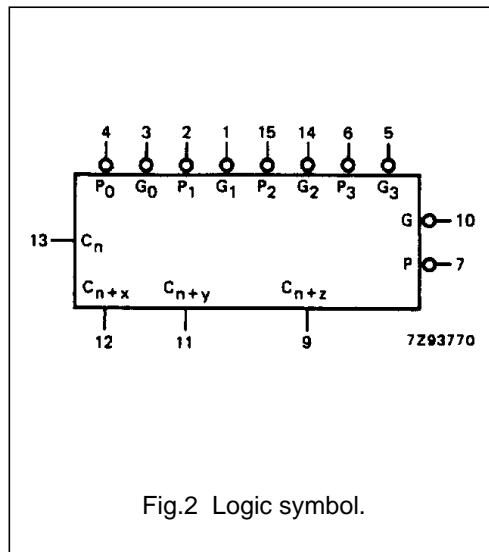
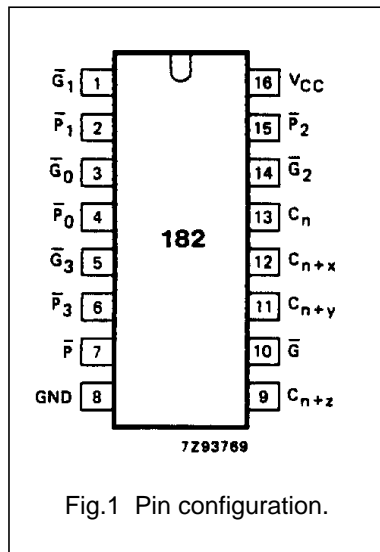
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# Look-ahead carry generator

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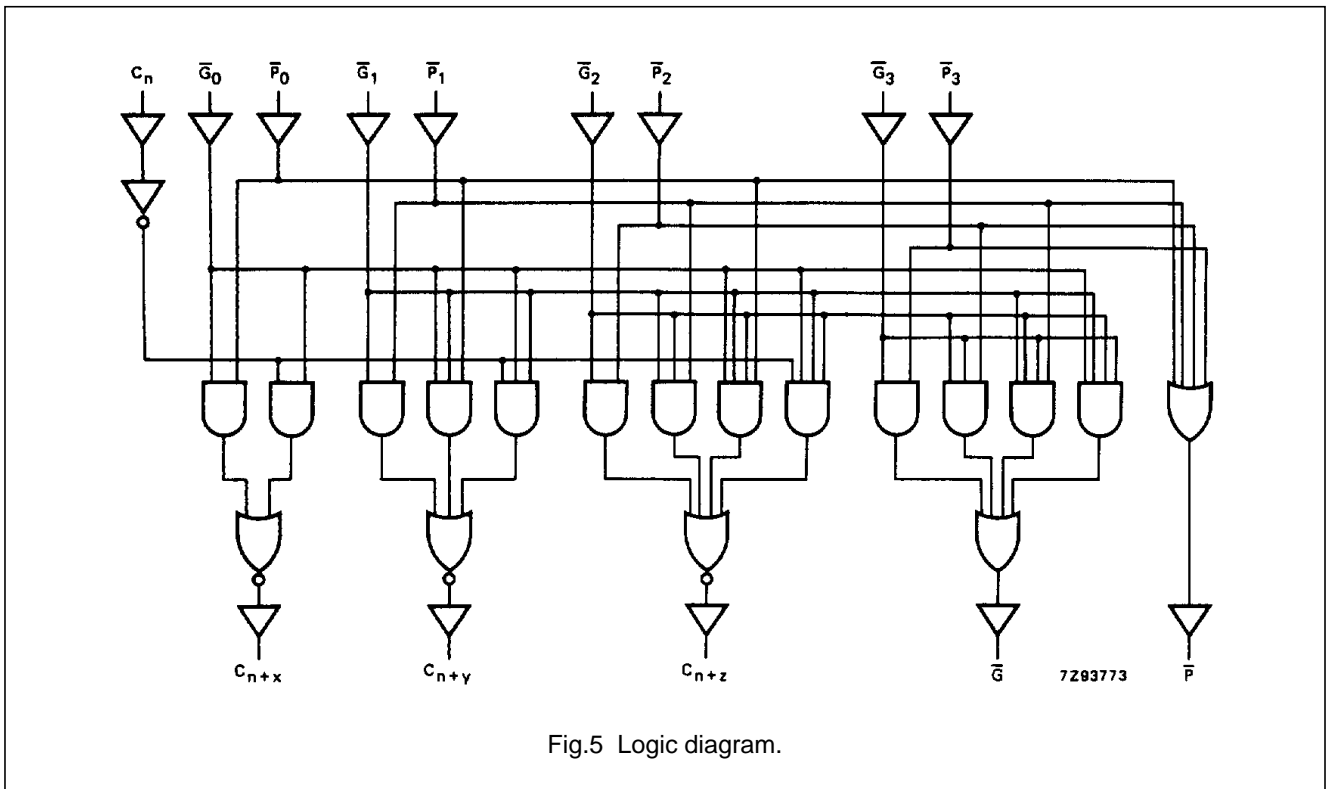
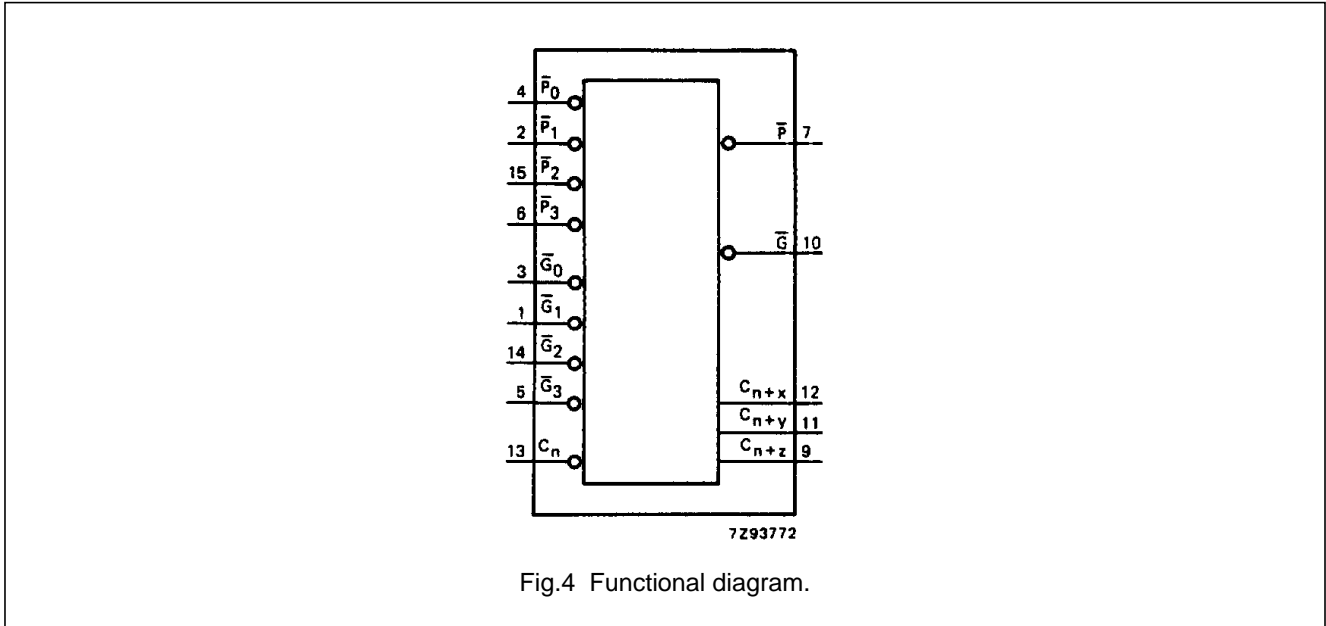
## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 1, 14, 5	$\overline{G}_0$ to $\overline{G}_3$	carry generate inputs (active LOW)
4, 2, 15, 6	$\overline{P}_0$ to $\overline{P}_3$	carry propagate inputs (active LOW)
7	$\overline{P}$	carry propagate output (active LOW)
8	GND	ground (0 V)
9	$C_{n+z}$	function output
10	$\overline{G}$	carry generate output (active LOW)
11	$C_{n+y}$	function output
12	$C_{n+x}$	function output
13	$C_n$	carry input (active HIGH)
16	$V_{CC}$	positive supply voltage



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FUNCTION TABLE

INPUTS									OUTPUTS				
$C_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$C_{n+x}$	$C_{n+y}$	$C_{n+z}$	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							L				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						L			
X	L	X	X	L						L			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
X	X	X	X	X	X	X	L	X			L		
X	X	X	L	X	X	L	X	L			L		
X	L	L	X	L	X	L	X	L			L		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

## Notes

1. H = HIGH voltage level  
L = LOW voltage level  
X = don't care

## Look-ahead carry generator

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{P}_n$ to $\overline{P}$		30 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay C <sub>n</sub> to any output		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{P}_n$ to $\overline{G}$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{P}_n$ to C <sub>n+n</sub>		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{G}_n$ to C <sub>n+n</sub>		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{G}_n$ to $\overline{G}$		41 15 12	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

## Look-ahead carry generator

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{G}_0, \overline{G}_1, \overline{P}_0, \overline{P}_1, \overline{P}_2$	1.50
$\overline{G}_3$	0.30
$\overline{G}_2, \overline{P}_3, C_n$	1.25

**AC CHARACTERISTICS FOR 74HCT**

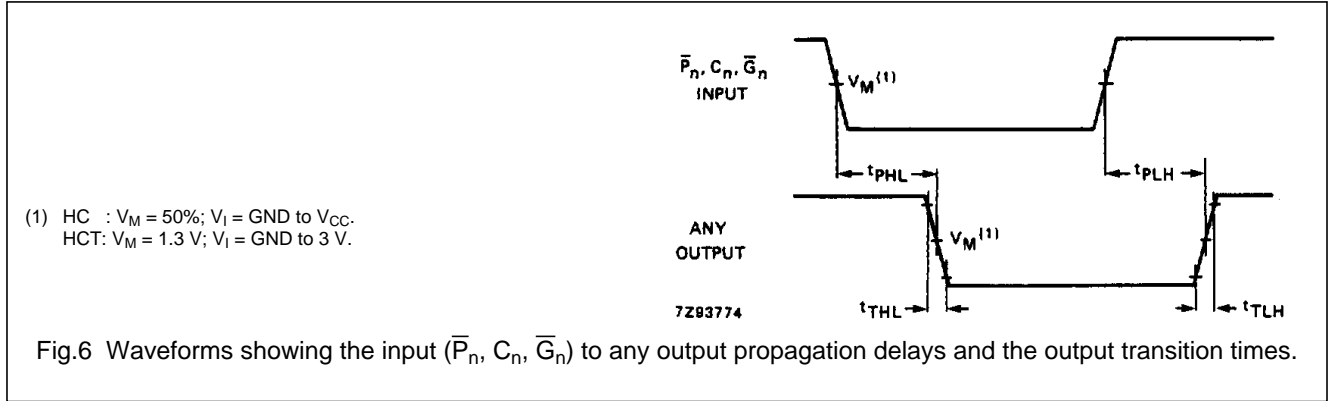
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)							UNIT	TEST CONDITIONS	
		74HCT								$V_{CC}$ (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
$t_{PHL} / t_{PLH}$	propagation delay $\overline{P}_n$ to $\overline{P}$		17	28		35		42	ns	4.5	Fig.6
$t_{PHL} / t_{PLH}$	propagation delay $C_n$ to any output		26	43		54		65	ns	4.5	Fig.6
$t_{PHL} / t_{PLH}$	propagation delay $\overline{P}_n$ to $\overline{G}$		20	33		41		50	ns	4.5	Fig.6
$t_{PHL} / t_{PLH}$	propagation delay $\overline{P}_n$ to $C_{n+n}$		20	33		41		50	ns	4.5	Fig.6
$t_{PHL} / t_{PLH}$	propagation delay $\overline{G}_n$ to $C_{n+n}, \overline{G}_n$ to $\overline{G}$		18	32		40		48	ns	4.5	Fig.6
$t_{THL} / t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig.6

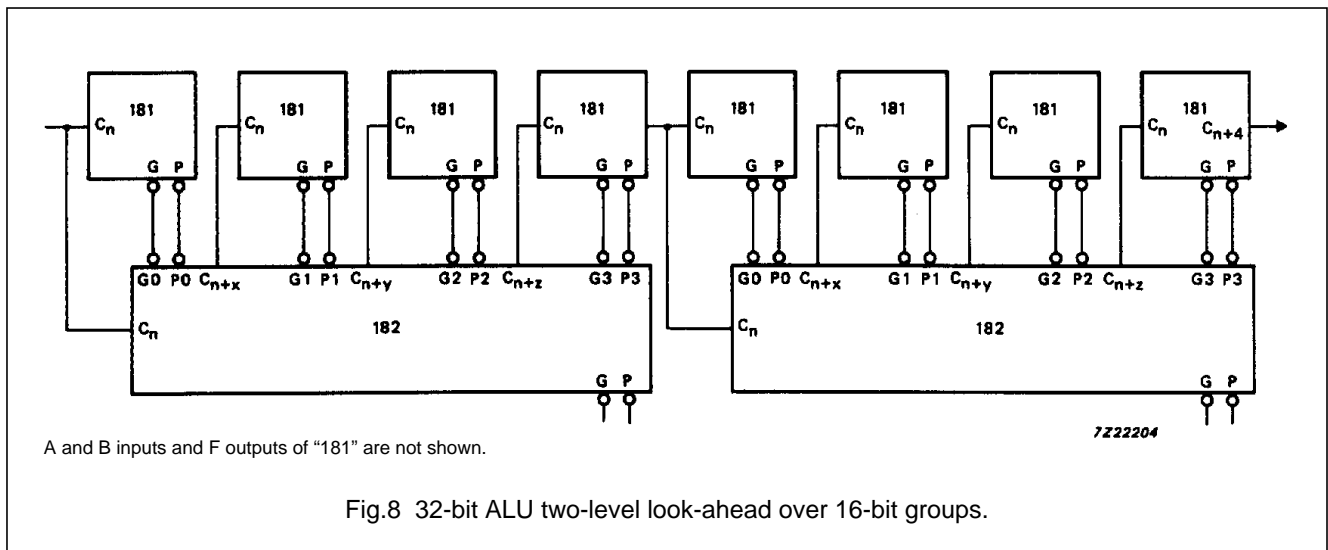
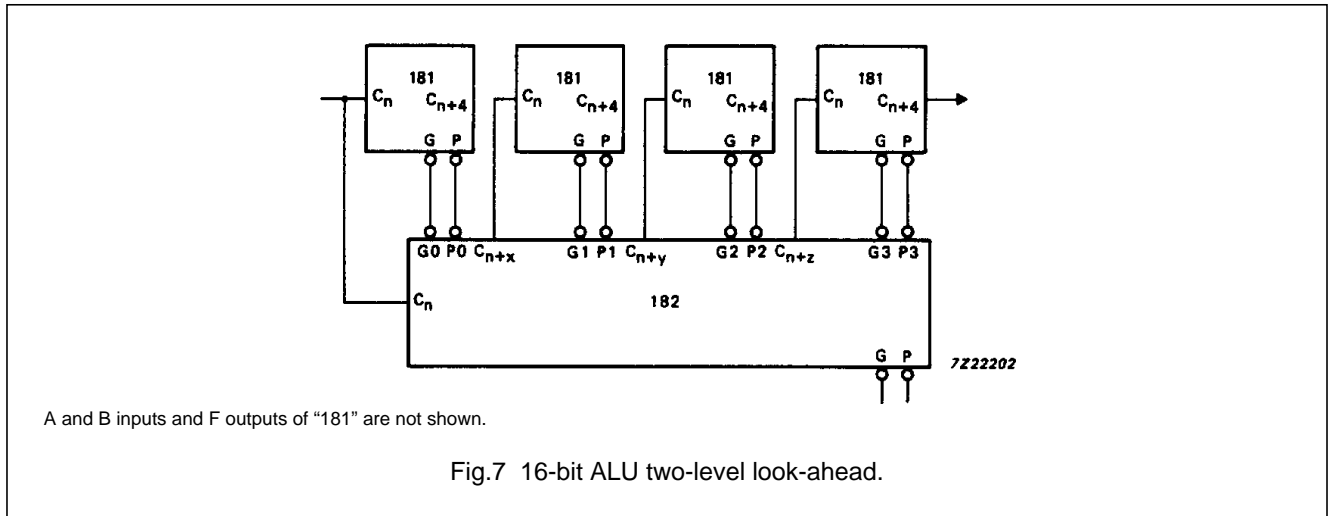
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## AC WAVEFORMS



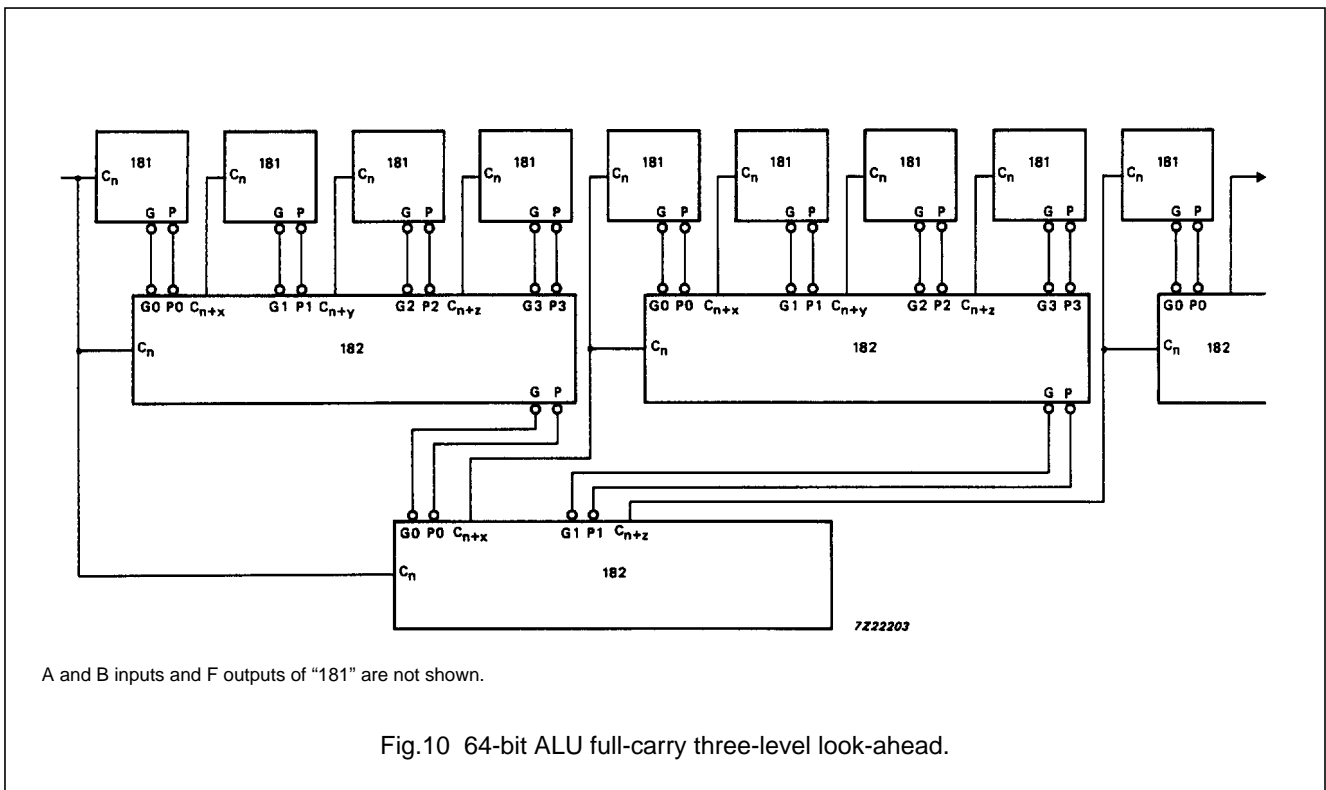
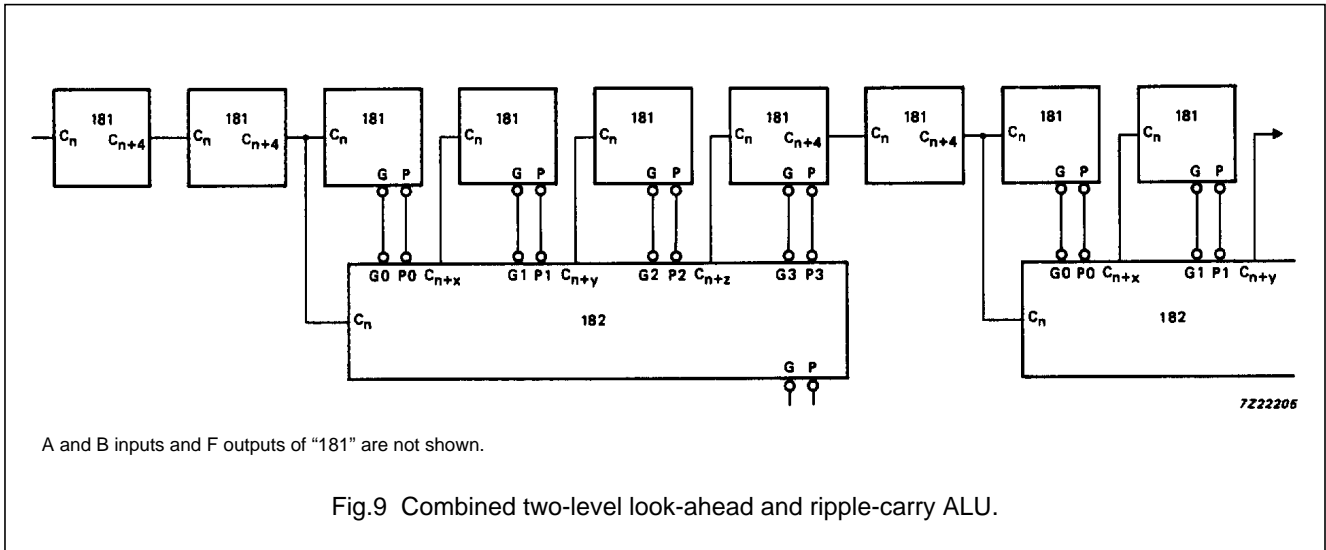
## APPLICATION INFORMATION





# Look-ahead carry generator

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## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".