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System-Engineering approach for the ITER PCS design: The correction coils current controller case study

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ABSTRACT

The Plasma Control System (PCS) is in charge of robustly controlling the evolution of plasma parameters against model uncertainties and disturbances, with the aim of achieving the envisaged goals and performance. The PCS design process follows a System-Engineering approach to support all the design phases, from control algorithms specifications to the verification and validation tests for various components. A case study concerning the design of the Correction Coils Current Controllers is presented in this paper. The aim is to show on a smaller scale the approach that is applied to the entire design of the PCS, by highlighting its effectiveness, from the refinement of the requirements, up to their validation in the simulation environment.

1. Introduction

The Plasma Control System (PCS) is a key component of the ITER tokamak, since it is in charge of robustly controlling the evolution of plasma parameters against model uncertainties and disturbances, with the aim of achieving the envisaged goals and performance [1]. As part of the PCS design activity, a System-Engineering (SE) approach was specified to support the design process itself [2]. Indeed, the PCS design includes many different aspects, which are not only limited to the specification of control algorithms, but includes also the definition of the verification and validation (V&V) tests for various components, as well as the commissioning procedures. Moreover, contributions to the design come from different parties that adopt heterogeneous sources. Hence, the adoption of the SE approach aims at aiding the management of such a complex process, and it has been adopted on top of the standard ITER life cycle, to homogenize and to keep track of the PCS design. Moreover, the proposed approach strongly relies on two software components: the PCS Database (PCSDB, [2,3]), implemented by using Enterprise Architect, and the PCS Simulation Platform (PCSSP, [4]), which exploits the Matlab/Simulink environment.

This paper deals with the case study of the Correction Coils (CC) Current Controllers design, which is used to show, on a smaller scale, what is applied to the entire design of the PCS. It highlights the effectiveness of the SE approach in supporting the PCS design, from the refinement of the requirements, up to their validation within the PCS Simulation Platform (PCSSP).

The CC are the set of 18 ex-vessel superconductive coils shown in Fig. 1, 6 bottom coils, 6 side coils and 6 top ones. These coils are connected in pairs, as shown in Fig. 2, in order to obtain 9 independent circuits fed by dedicated power supplies. These coils will be used to compensate the unavoidable small non-axisymmetric magnetic fields that may cause tearing modes to grow, and therefore disruptions. It is worth notice that, due to the way the coils are connected, they are naturally decoupled from perfect axisymmetric current sources, therefore they should not affect the plasma axisymmetric magnetic control system [5]. During the Engineering Operation (EO) phase, which is planned after the First Plasma one [1], it is envisaged to use the CC to track pre-computed current waveforms (feedforward control), rather than performing closed-loop control of the error field. Therefore the current control mode is needed for the CC during EO.

In this paper we first show how a set of system and performance requirements are derived by starting from the high-level ones stored in the PCSDB, which are typically either qualitative or too generic to be used to guide the design of a control system. The CC current controller is then designed to satisfy both the functional and performance (non-functional) requirements. The control algorithm design phase is carried out with the PCSSP and documented in the PCSDB. As it will be shown,

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Table 1
Performance requirements for the CC current controller in the EO phase.

Name	Description
CC Current Control maximum overshoot	The PCS shall be able to simultaneously control currents in the CC such that the maximum overshoot for a step response is less than 20%
CC Current Control settling time	The PCS shall be able to simultaneously control currents in the CC with a settling time < 5 s
CC Current Control tracking error performance	The PCS shall be able to simultaneously control currents in the CC such that the maximum steady state error when tracking a ramp with slope equal to SL is $< 0.02SL$
CC Current Control Ramp Rate performance	The PCS shall control the current in the CC with a current ramp rate of at least 1 kA/s

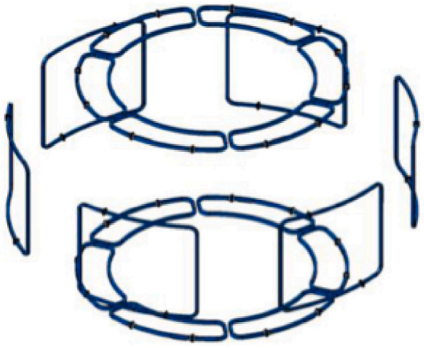

Fig. 1. The 18 ITER superconductive Correction Coils (CC). The coils are placed at three different vertical positions.

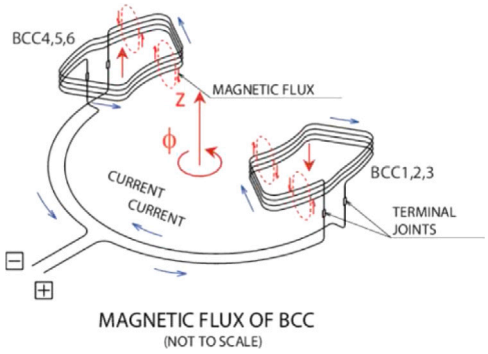

Fig. 2. Schematic of the connection of two bottom CC.

it turns out that a set of Proportional and Integral (PI) regulators is sufficient to robustly achieve the performance required to support EO of the CC. Finally, by starting from the performance requirements, a set of test cases are derived and used to assess the controller performance as part of the V&V process. Such a performance assessment is performed by running specific simulations in the PCSSP environment, whose results are eventually documented in the PCSDB. As a result, the PCSDB holds all the relevant information to track the design of the CC current controller and to support its final implementation on the real-time target framework [6].

The next sections are devoted to detail each of the phases introduced above.

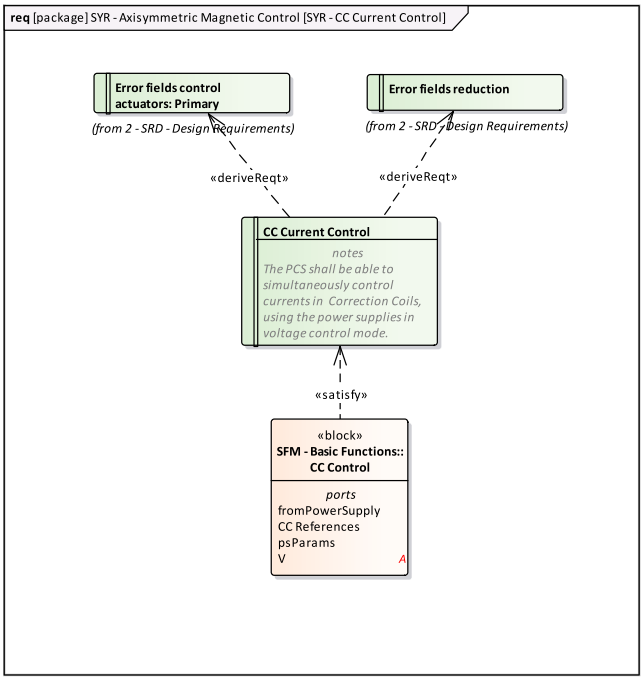

Fig. 3. SYR requirements for the CC Control block and its relation with SRD requirements.

2. Requirements for the current control of the ITER CC

Following the design methodology adopted for the design of the PCS [2,3] the system requirements for the EO phase are derived starting from the high-level ones specified in the ITER System Requirement Document (SRD) of the PCS. The content of the latter document has been imported in the PCSDB, which allows to easily extract information. Indeed, from the PCSDB the following two SRD requirements have been identified as relevant for EO:

- **Error fields control actuator (primary)** *"The primary actuators to control error fields shall include error field correction coils and their power supplies"*
- **Error fields reduction:** *"The PCS shall be required to be capable of reducing error fields"*

High-level requirements from the SRD do not necessarily identify a function to be implemented in the PCS. Aiming at identifying such functions, which will then be mapped to architectural components,

Table 2
PI gains of the CC control block.

Proportional gain K_P	2.55
Integral gain K_I	0.36

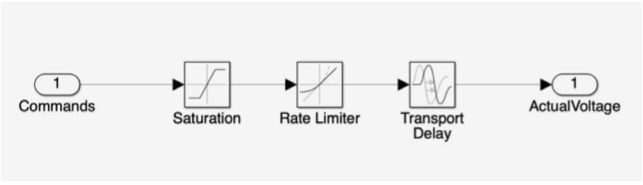

Fig. 4. CC power supply model used for performance assessment.

the adopted methodology requires to derive *system-oriented operative* requirements, *SYRs* in the ITER PCS jargon. For the EO phase, the following SYR has been derived starting from the above listed SRD requirements.

- *"The PCS shall be able to simultaneously control currents in Correction Coils, using the power supplies in voltage control mode"*

where *simultaneity* refers to the fact that the case in which all the CC are simultaneously energized must be considered. Indeed, due to residual coupling, the current flowing in each pair of coils acts as a disturbance to be rejected on the other CC circuits.

The next design phase leads to the identification of the *CC Control* functional block, which is the control function to be implemented within the PCS. The diagram reported in Fig. 3 summarizes the relationships between SRD, SYR and the CC control block, as modelled within the PCSDB. By means of *port* objects, the functional block definition also specifies the interface with diagnostics and/or plant systems and/or other PCS components. Other than specifying the interface, the *ports* map the various input and output signals with the ones specified in the so called *Interface Sheets*, i.e. the ITER documents that specify interface requirements and constraints that the PCS imposes on other plant systems, and vice versa. Once functional block are used to model the PCS components, the internal connection between such components is further detailed by using Internal Block Diagrams (IBDs, [7]). As a result, this design phase permits to verify the interface, as well as to identify possible missing signals.

As for the *CC Control* block, two input vectors are required: the reference waveforms for the current in each CC circuit (*CC References* in Fig. 3), and the correspondent current measurements (which is contained in the *psParams* structure, also reported in Fig. 3). The output vector contains the voltage requests to each CC power supply (the *V* port in Fig. 3). Since during the EO phase the CC will be not used to perform error field control, no connections with other PCS components is envisaged. The reader interested to how IBDs can be used to model the PCS internal structure can refer to the case of PCS for *First Plasma* described in [2].

However, although the derived SYR allows to identify the function to be implemented to control the current in the CC and its interface, it is not sufficient to assess the performance. To this aim, by discussing with all the stakeholders involved, i.e. the responsible officers for the CC, the power supplies and the PCS, the non functional performance requirements for the EO phase listed in Table 1 have been derived from the identified SYR. Such non functional requirements allows the CC current controller to track the envisaged reference waveforms for EO, by taking into account also the constraints on the maximum output voltage of the CC power supplies.

3. Design of the CC current control

Starting from the performance requirements introduced in the previous section, the CC current control block has been designed exploiting

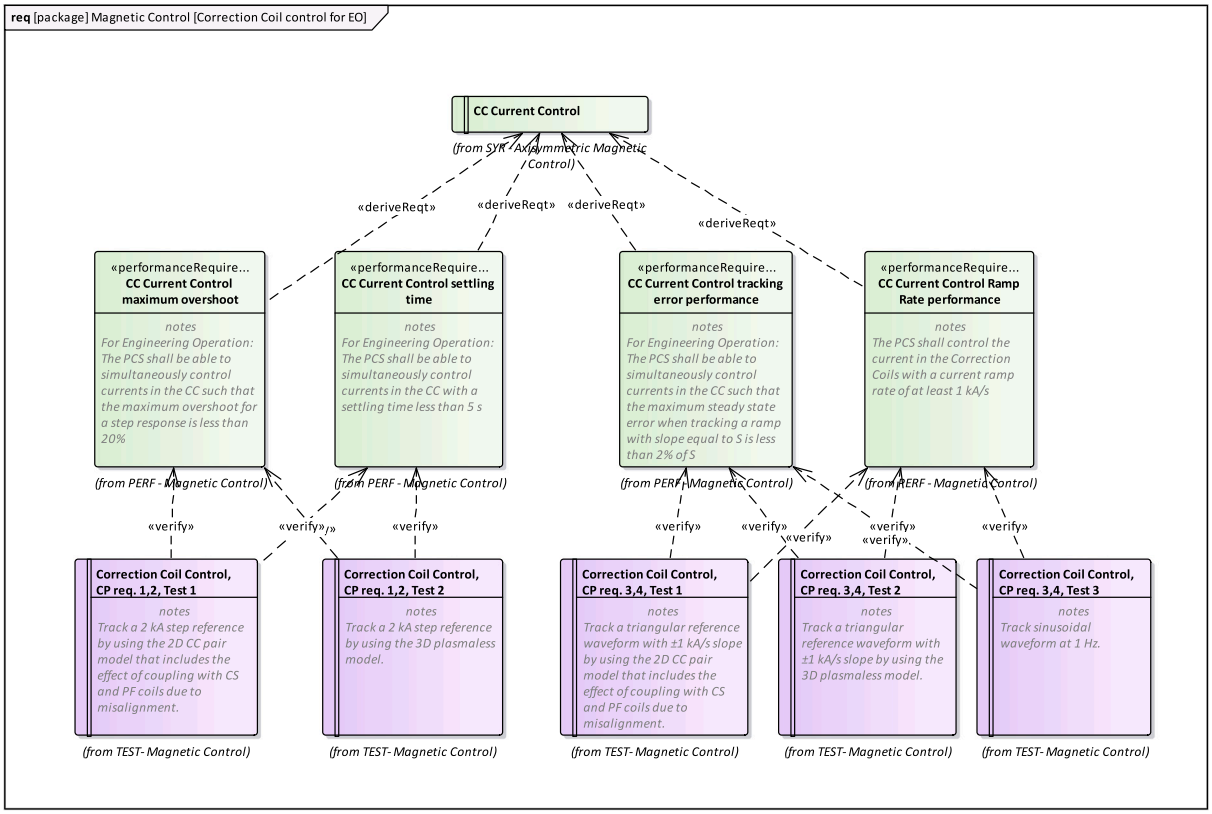

Fig. 5. Test cases and their relationships with Performance Requirements listed in Table 1.

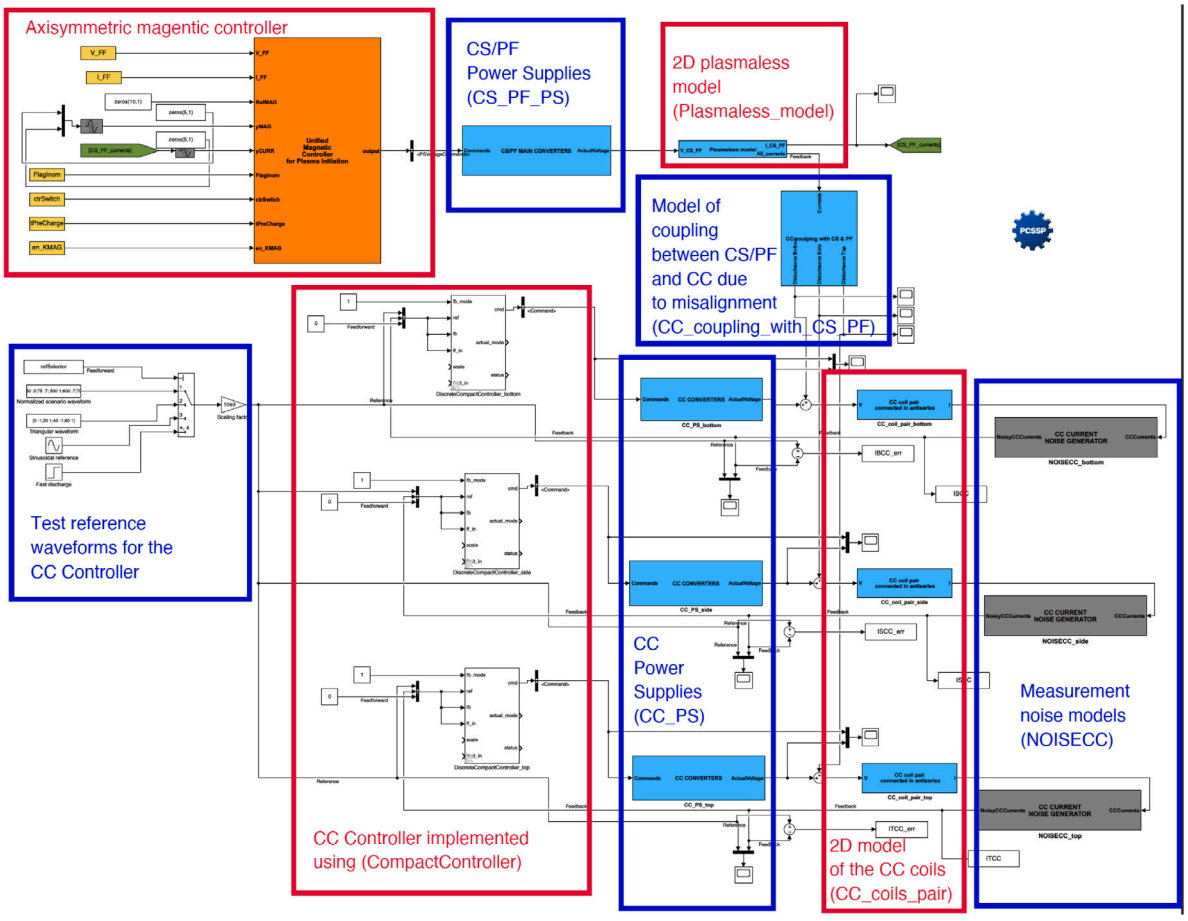

Fig. 6. Simulink PCSSP-compliant model used to run the simulations that correspond to the Test cases no. 1 and no. 2 reported in Table 3.

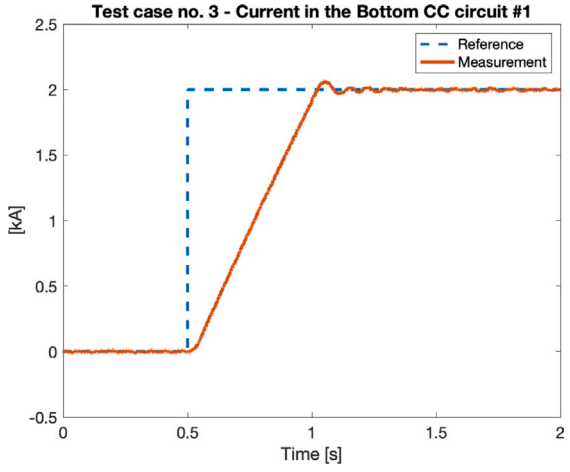

Fig. 7. Current in Bottom CC circuit for Test case no. 3.

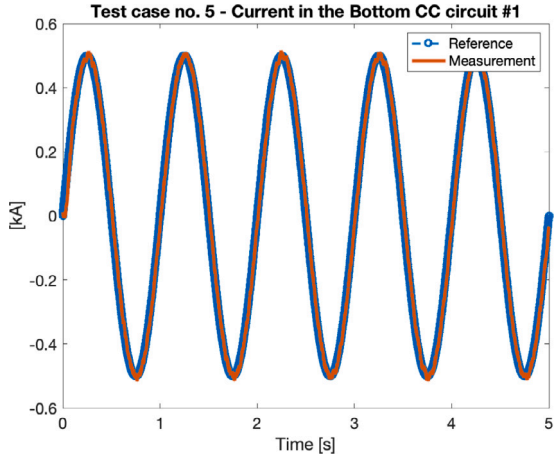

Fig. 8. Current in Bottom CC circuit for Test case no. 5.

simple *design-oriented* models for both the coils and the power supplies. As for the CC, each has been modelled as a LR circuit obtained by connecting two symmetric coils in antiseries. Therefore, as for the design, the coupling among the different pairs has been neglected, as well as the coupling with the ITER CS and PF coils.

Moreover, a very simple model of the CC power supply consisting of a 5 ms pure delay has been considered; such a choice for the delay should represent the worst case.

Since the performance requirements listed in Table 1 mainly refer to the tracking of piecewise linear reference waveforms, a Proportional–Integral (PI) structure has been chosen for the CC control block, whose control law is given by

$$V_{req}(t) = K_P\left(I_{ref}(t) - I_{meas}(t)\right) + K_I \int_0^t \left(I_{ref}(\tau) - I_{meas}(\tau)\right) d\tau\,, \quad (1)$$

Table 3
Test cases for the assessment of the CC control block.

No.	Description	Covered requirements
1	Track a 2 kA step reference by using the 2D CC pair model that includes the effect of coupling with CS and PF coils due to misalignment	CC Current Control maximum overshoot – CC Current Control settling time
2	Track a triangular reference waveform with ±1 kA/s slope by using the 2D CC pair model that includes the effect of coupling with CS and PF coils due to misalignment	CC Current Control tracking error performance – CC Current Control Ramp Rate performance
3	Track a 2 kA step reference by using the 3D plasmaless model	Current Control maximum overshoot – CC Current Control settling time
4	Track a triangular reference waveform with ±1 kA/s slope by using the 3D plasmaless model	CC Current Control tracking error performance – CC Current Control Ramp Rate performance
5	Track sinusoidal waveform at 1 Hz	CC Current Control tracking error performance – CC Current Control Ramp Rate performance

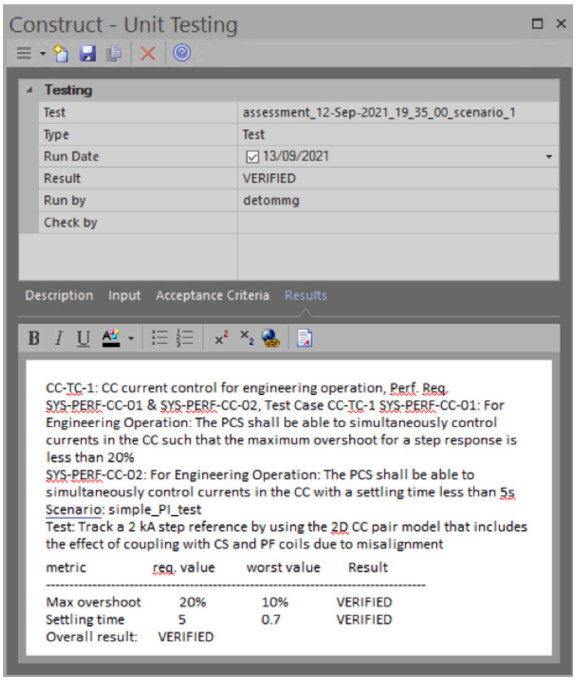

Fig. 9. Assessment results stored in PCSDB.

where $V_{req}(t)$ is the voltage request to the CC power supply, $I_{ref}(t)$ is the current reference for the current in the CC pair connected in antiseries, $I_{meas}(t)$ is the measured current flowing in the CC pair, while K_P and K_I are the proportional and integral gains of the CC control block, respectively. The design of these gains has been carried out exploiting the above mentioned simplified models of both the CC pairs and power supply. More in details, a single set of gains has been designed for all the CC pairs, i.e. the controller parameters are the same for the current controller of the bottom, side and top CC shown in Fig. 1. The designed values are reported in Table 2.

4. Prototyping in PCSSP and performance assessment

This section first briefly introduces the PCSSP modules that have been developed to prototype the CC control block and to model the plant behaviour. All these modules are available in the PCSSP-ITER git repository [8]. In the second part of the section, the test cases considered for to assess the performance requirements reported in Table 1 are presented, together the simulation results.

4.1. PCSSP modules

As for the CC control block, this has been prototyped in PCSSP by using the *CompactController* configurable block [9]. Indeed, the PI control law (1) is one of the CompactController available control modes; therefore the behaviour of the CC control block is obtained by simply configuring this general purpose one.

Moreover, to perform the required assessments in PCSSP, the following modules have been developed to model the plant behaviour:

- `CC_PS`; models the CC power supplies as the cascade of (see also Fig. 4)
  - a saturation, that accounts for the power supply maximum voltage $V_{\max}$;
  - a rate limiter, whose value has been set equal to
    $$SR = \frac{V_{\max}}{40 \cdot 10^{-3}},$$
    i.e., it has been assumed the worst case scenario, where 40 ms are needed to swing from 0 V to the maximum voltage;
  - a 5 ms pure delay.
- `CC_Coil_pair`; models the behaviour of a single CC pair connected in antiseries as an LR circuit. It takes the voltage applied to the circuit as input, while it returns the corresponding current as output.
- `Plasmaless_model`; models the coupled behaviour of the CS and PF coils in absence of plasma under 2D axisymmetric assumptions. Similar to the previous module, it takes the voltages applied to the coils as input and returns the corresponding currents.
- `CC_coupling_with_CS_PF`; generates additional voltages to be applied as disturbances input the CC pairs. These voltages simulates the coupling between the CS/PF coils and the CC pairs, due to a misalignment of the latter. It requires the current flowing in the CS and PF coils as input.
- `Plasmaless_model_3D`; models the behaviour of the currents in the CS, PF and CC circuits in absence of plasma.
- `NOISECC`; models the noise on the CC current measurements.

4.2. Test cases and performance assessment

The test cases reported in Table 3 have been defined to cover the assessment of the performance requirements introduced in Section 2. The corresponding relationships modelled in the PCSDB are shown by the diagram in Fig. 5. All the test cases have been run in PCSSP, the Matlab/Simulink based simulation platform developed to support the design of the ITER PCS [4].

The Simulink model reported in Fig. 6 is the one that has been used to run the Test cases no. 1 and no. 2 reported in Table 3. In this case, a single 2D model of the CC (implemented by the `CC_Coil_pair`) has been considered for each vertical position – bottom, side and top – although the residual coupling due to misalignment with the axisymmetric superconductive CS/PS coils has been considered. In particular, the CS/PF current controller developed for the First Plasma phase has been used to track the breakdown waveforms. This control has been closed on a 2D plasmaless model of the CS and PF coils (the `Plasmaless_model` PCSSP module), and the simulated CS/PF are fed as inputs to the *ad hoc* PCSSP module that models the residual coupling. Such module generate, as output, additional voltages that are added as disturbances to the *CC Controller* requests. Moreover, it is worth to notice that the CC Controller for the various circuits (bottom, side and top) are simultaneously fed with the same reference waveforms, in accordance with the SYR introduced in Section 2.

As an example of assessment results, Fig. 7 shows the step response for Test case no. 3: it can be seen that the performance requirements on both the maximum overshoot and on the sampling time are met. Furthermore, Fig. 8 show the result of Test case no. 5, that shows the capability of the CC control block to track a 1 Hz sinusoidal waveform.

According to the adopted methodology, all the assessment results have been imported in the PCSDB. Fig. 9 shows an example assessment result as stored in the PCSDB.

5. Conclusions

The ITER PCS design team has adopted a SE approach to document and trace the various phase PCS development. This paper considered the current control for the CC case study to describe each stage of the proposed methodology. The same approach is currently adopted to design the PCS functions needed during the PFPO-1 phase.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgement

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